High Performance, 4-/8-Channel, Fault-Protected Analog Multiplexers

ADG438F/ADG439F

FEATURES

All switches off with power supply off
Analog output of on channel clamped within power supplies if an overvoltage occurs
Latch-up proof construction
Fast switching times
t_{ON} 250 ns maximum
t_{OFF} 150 ns maximum
Fault and overvoltage protection: −40 V to +55 V
Break-before-make construction
TTL- and CMOS-compatible inputs

APPLICATIONS

Data acquisition systems
Industrial and process control systems
Avionics test equipment
Signal routing between systems
High reliability control systems

GENERAL DESCRIPTION

The ADG438F and ADG439F are CMOS analog multiplexers, with the ADG438F comprising eight single channels and the ADG439F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, and n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from −40 V to +55 V. During fault conditions with power supplies off, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current flows. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG438F switches one of eight inputs to a common output as determined by the 3-bit binary address lines, A0, A1, and A2. The ADG439F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines, A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off.

FUNCTIONAL BLOCK DIAGRAM

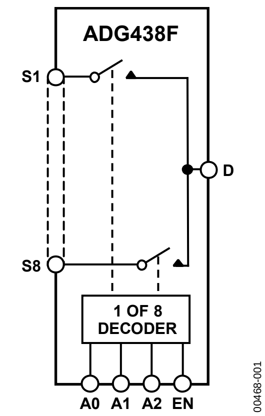

Figure 1.

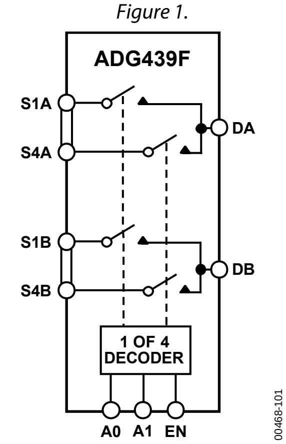

Figure 2.

PRODUCT HIGHLIGHTS

1. Fault Protection. The ADG438F and ADG439F can withstand continuous voltage inputs up to −40 V or +55 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. On channel saturates while fault exists.
3. Low R_{ON}.
4. Fast Switching Times.
5. Break-Before-Make Switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Eliminates Latch-Up. A dielectric trench separates the p-channel and n-channel MOSFETs thereby preventing latch-up.
7. Improved Off Isolation. Trench isolation enhances the channel-to-channel isolation of the ADG438F/ADG439F.

Rev. E

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version +25°C	−40°C to +85°C	−40°C to +105°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range	V_{SS} + 1.4				V typ	Output open circuit
	V_{DD} − 1.4				V typ	
	V_{SS} + 2.2				V typ	Output loaded, 1 mA
	V_{DD} − 2.2				V typ	
R_{ON}	270				Ω typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA
		390	420	450	Ω max	See Figure 17
On-Resistance Flatness, $R_{FLAT (ON)}$	9				% typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA
	10	10	10	10	% max	
R_{ON} Drift	0.6				%/°C typ	V_S = 0 V, I_S = 1 mA
On-Resistance Match Between Channels, ΔR_{ON}	3	3	3	3	% max	V_S = ±10 V, I_S = 1 mA
LEAKAGE CURRENTS						
Source Off Leakage, I_S (Off)	±0.01				nA typ	V_D = ±10 V, V_S = ∓10 V
	±0.5	±1.5	±1.5	±4	nA max	See Figure 18
Drain Off Leakage, I_D (Off)	±0.01				nA typ	V_D = ±10 V, V_S = ∓10 V
ADG438F ADG439F	±0.5	±5	±5	±20	nA max	See Figure 19
Channel On Leakage, I_D, I_S (On)	±0.01				nA typ	V_S = V_D = ± 10 V
ADG438F/ADG439F	±0.5	±5	±5	±20	nA max	See Figure 20
FAULT						
Source Leakage Current, I_S (Fault)	±0.02				nA typ	V_S = +55 V or −40 V, V_D = 0 V; see Figure 21
(With Overvoltage)	±0.05	±0.1	±0.2	±0.2	µA max	
Drain Leakage Current, I_D (Fault)	±0.05				nA typ	V_S = ±25 V, V_D = ∓10 V; see Figure 19
(With Overvoltage)	±0.05	±0.1	±0.2	±0.2	µA max	
Source Leakage Current, I_S (Fault) (Power Supplies Off)	±30				nA typ	V_S = ±25 V, V_D = V_{EN}, A0, A1, A2 = 0 V
	±0.1	±0.2	±0.3	1	µA max	See Figure 22
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8	0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Digital Input Capacitance, C_{IN}	5				pF typ	
DYNAMIC CHARACTERISTICS[1]						
$t_{TRANSITION}$	175				ns typ	R_L = 1 MΩ, C_L = 35 pF
	220	300	300	330	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; see Figure 25
t_{OPEN}	90					
	60	40	40	40	ns min	R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V; see Figure 26
t_{ON} (EN)	180				ns typ	R_L = 1 kΩ, C_L = 35 pF
	230	300	300	345	ns max	V_S = 5 V; see Figure 27
t_{OFF} (EN)	100				ns typ	R_L = 1 kΩ, C_L = 35 pF
	130	150	150	173	ns max	V_S = 5 V; see Figure 27

Parameter	B Version +25°C	−40°C to +85°C	−40°C to +105°C	−40°C to +125°C	Unit	Test Conditions/Comments
Settling Time, t_{SETT}						
0.1%		1	1	1	µs typ	R_L = 1 kΩ, C_L = 35 pF
0.01%		2.5	2.5	2.5	µs typ	V_S = 5 V
Charge Injection	15				pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	93				dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 V rms; see Figure 23
Channel-to-Channel Crosstalk	93				dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 rms; see Figure 24
C_S (Off)	3				pF typ	
C_D (Off)						
ADG438F	22				pF typ	
ADG439F	12				pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05				mA typ	V_{IN} = 0 V or 5 V
	0.1	0.2	0.2	0.2	mA max	
I_{SS}	0.1				µA typ	
		1	1	1	µA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Digital Input, EN, Ax	−0.3 V to V_{DD} + 0.3 V or 20 mA, whichever occurs first
V_S, Analog Input Overvoltage with Power On (V_{DD} = +15 V, V_{SS} = −15 V)	V_{SS} − 25 V to V_{DD} + 40 V
V_S, Analog Input Overvoltage with Power Off (V_{DD} = 0 V, V_{SS} = 0 V)	−40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Plastic DIP Package	
$θ_{JA}$, Thermal Impedance	117°C/W
SOIC Package	
$θ_{JA}$, Thermal Impedance	
Narrow Body	125°C/W
Wide Body	90°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

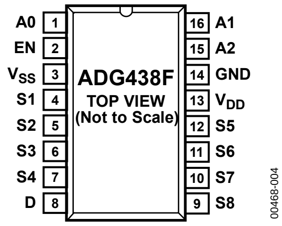

Figure 3. ADG438F Pin Configuration

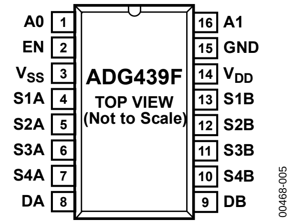

Figure 4. ADG439F Pin Configuration

Table 3. ADG438F Pin Function Description

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

Table 4. ADG439F Pin Function Description

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

Table 5. ADG438F Truth Table[1]

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = don't care.

Table 6. ADG439F Truth Table[1]

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

[1] X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

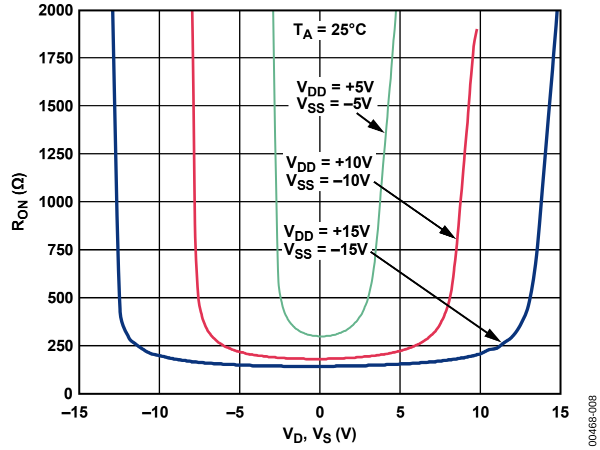

Figure 5. On Resistance as a Function of V_D (V_S)

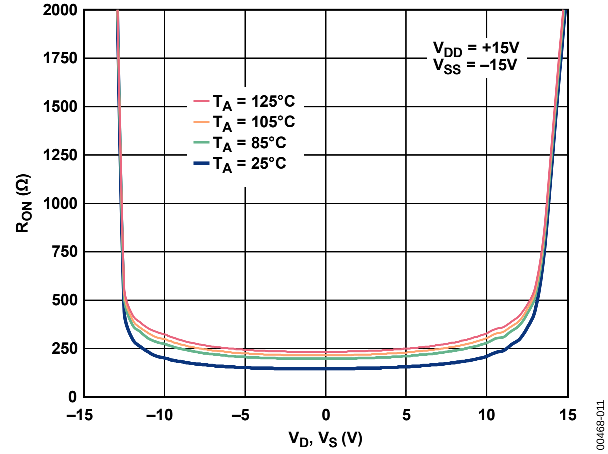

Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures

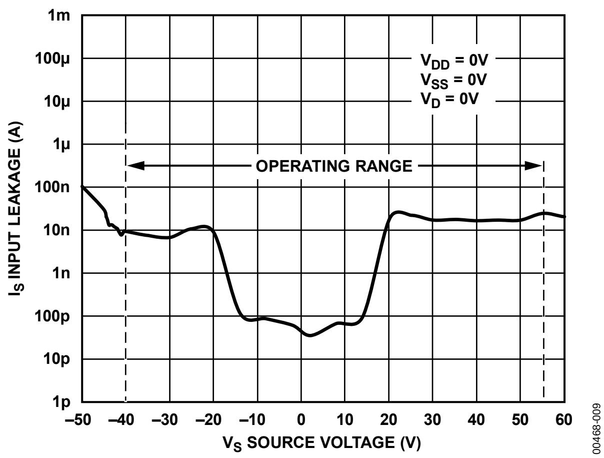

Figure 6. Source Input Leakage Current as a Function of V_S (Power Supplies Off) During Overvoltage Conditions

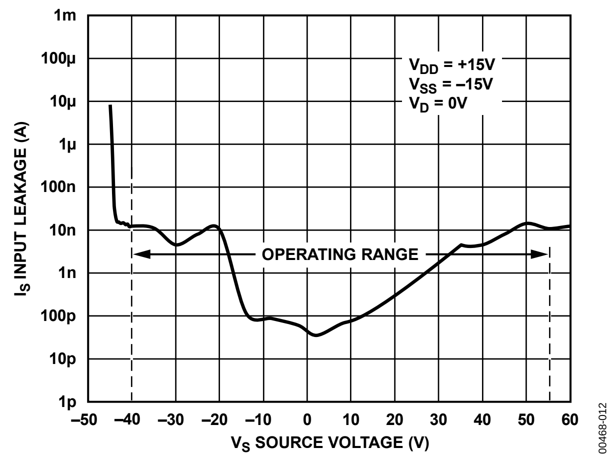

Figure 9. Source Input Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

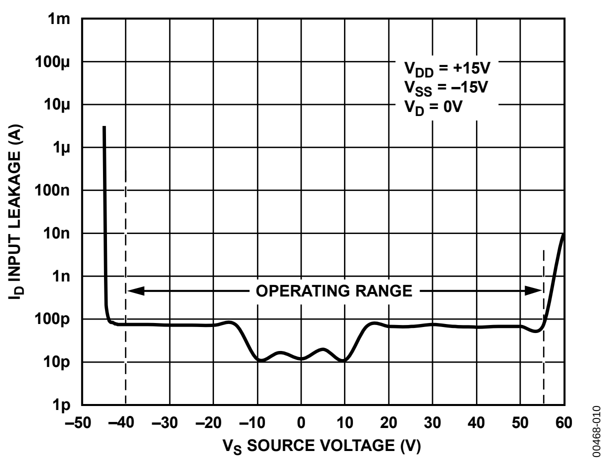

Figure 7. Drain Output Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

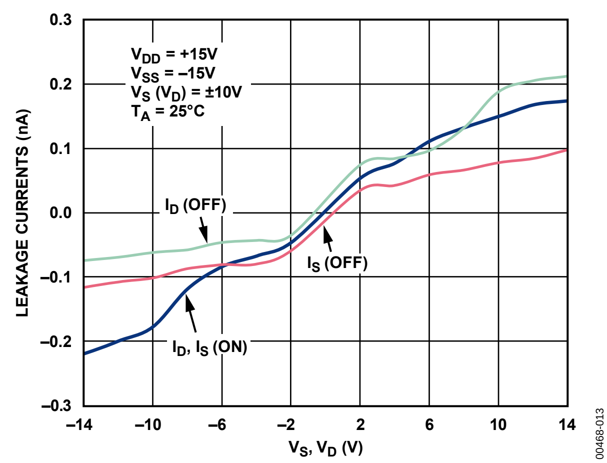

Figure 10. Leakage Currents as a Function of V_D (V_S)

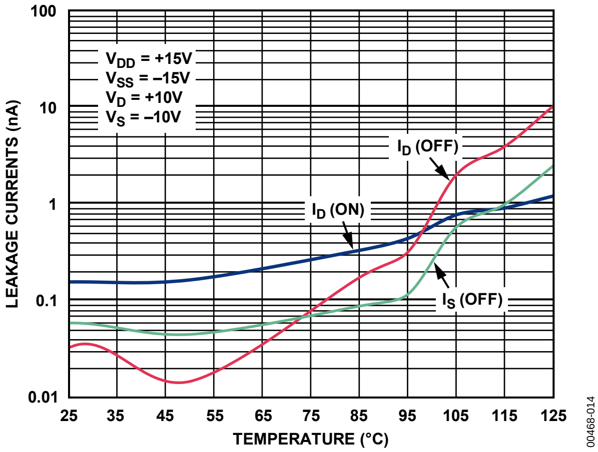

Figure 11. Leakage Currents as a Function of Temperature

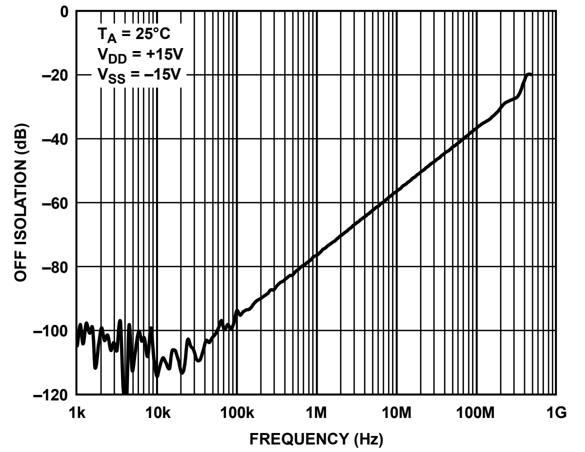

Figure 14. Off Isolation vs. Frequency, ±15 V Dual Supply

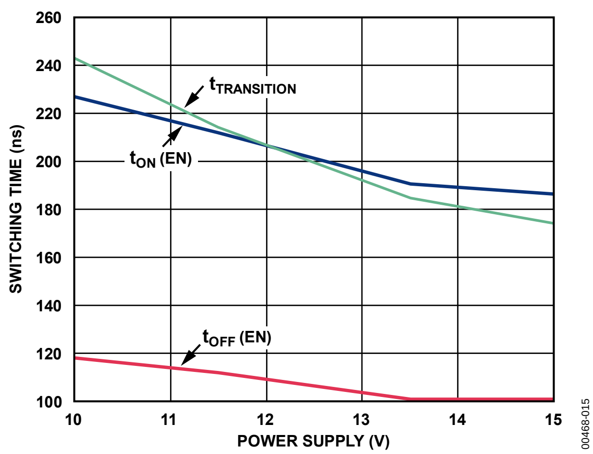

Figure 12. Switching Time vs. Dual Power Supply

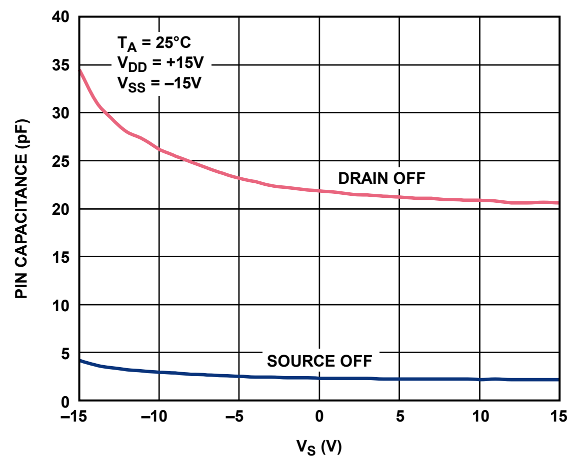

Figure 15. Capacitance vs. Source Voltage

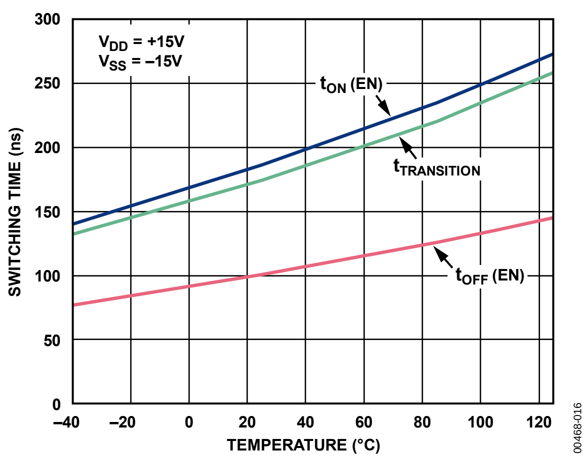

Figure 13. Switching Time vs. Temperature

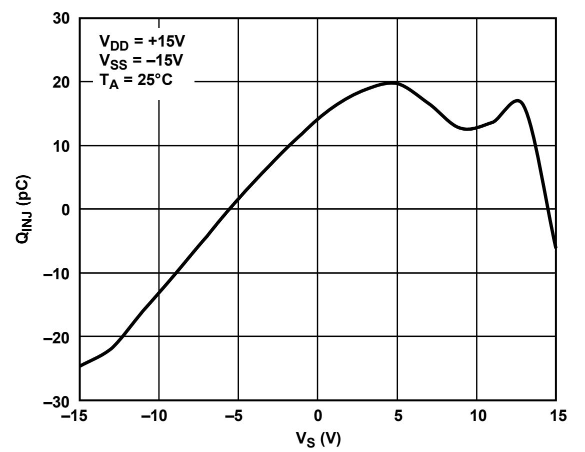

Figure 16. Charge Injection vs. Source Voltage

TEST CIRCUITS

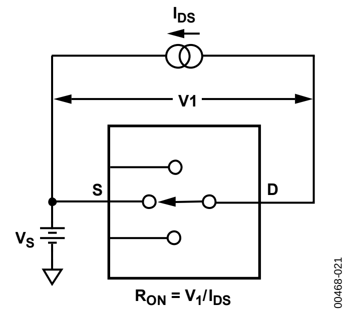

Figure 17. On Resistance

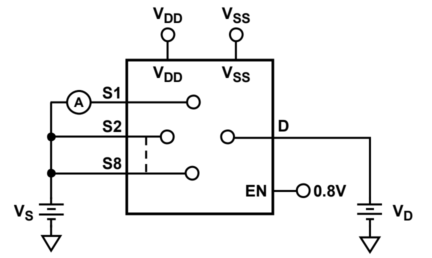

Figure 21. Input Leakage Current (with Overvoltage)

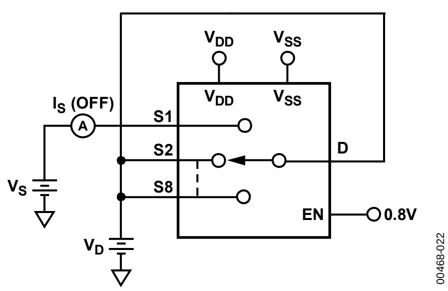

Figure 18. I_S (Off)

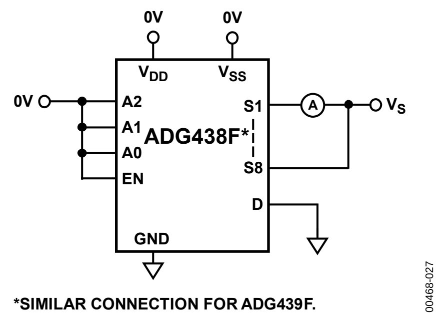

Figure 22. Input Leakage Current (with Power Supplies Off)

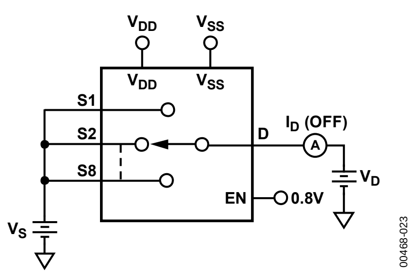

Figure 19. I_D (Off)

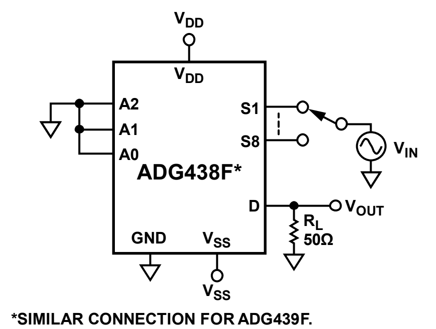

Figure 23. Off Isolation

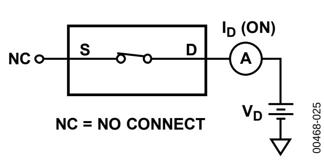

Figure 20. I_D (On)

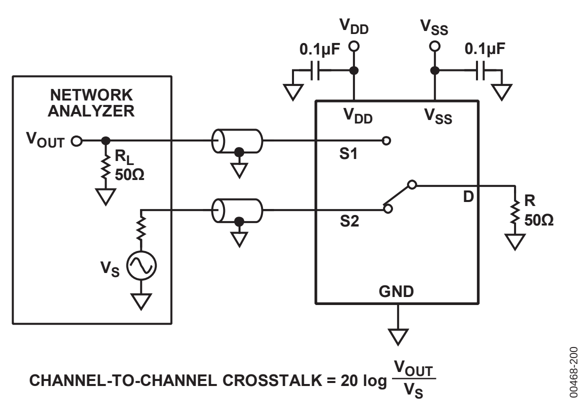

Figure 24. Channel-to-Channel Crosstalk

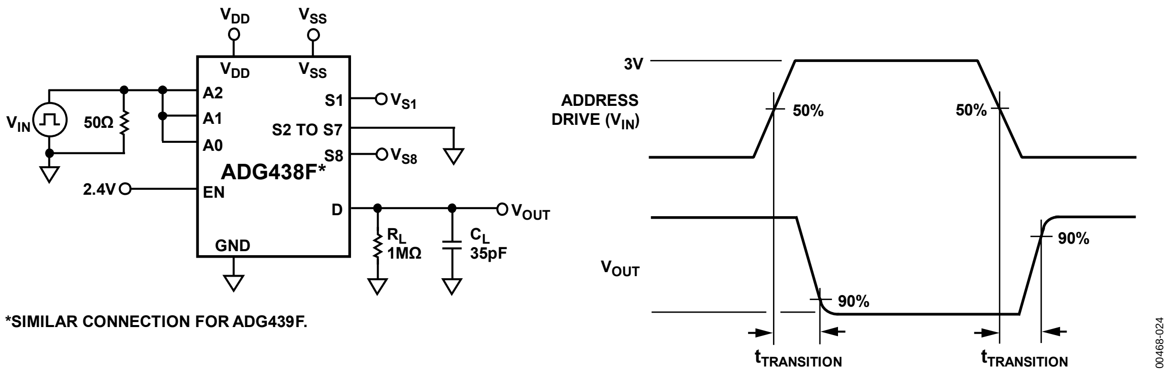

Figure 25. Switching Time of Multiplexer, $t_{TRANSITION}$

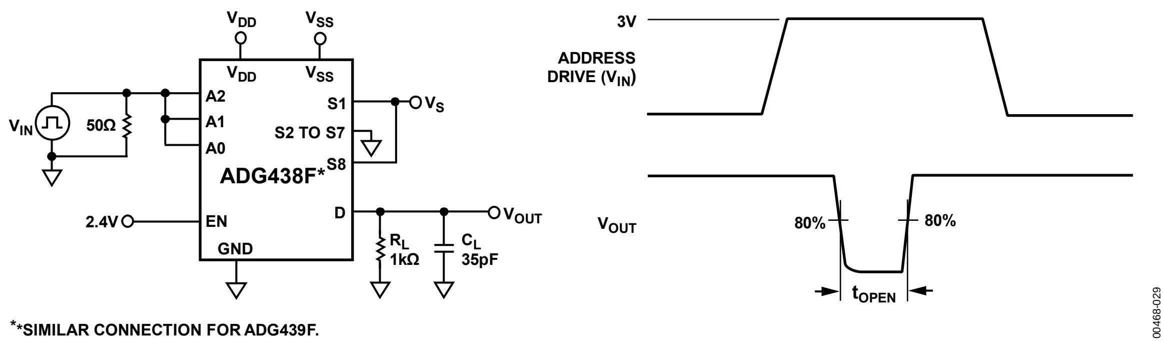

Figure 26. Break-Before-Make Delay, t_{OPEN}

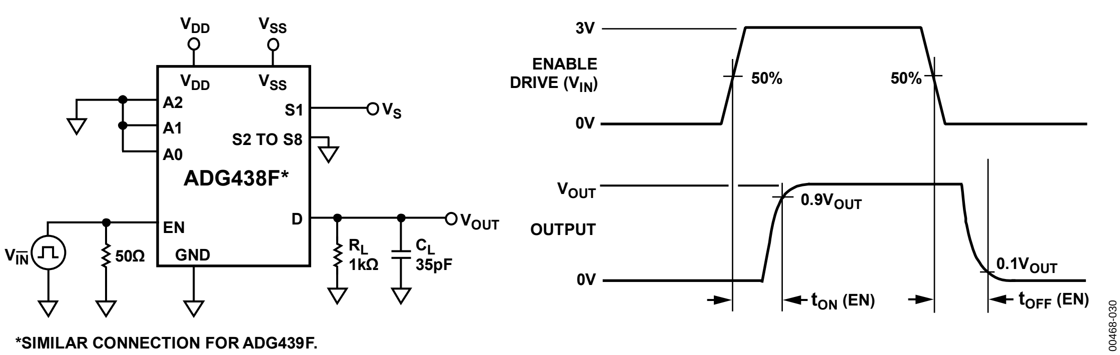

Figure 27. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

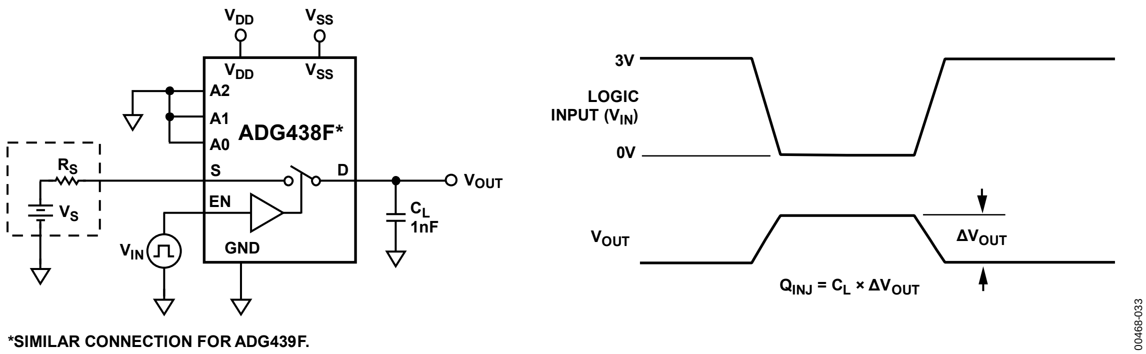

Figure 28. Charge Injection

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels as a percentage of the maximum R_{ON} of those two channels.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of the on resistance measured over the specified analog signal range and is represented by $R_{FLAT (ON)}$.

Flatness is calculated by

$$((R_{MAX} - R_{MIN}) / R_{MAX} \times 100)$$

R_{ON} Drift
Change in R_{ON} when temperature changes by one degree Celsius.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

I_S (Fault—Power Supplies On)
Source leakage current when exposed to an overvoltage condition.

I_D (Fault—Power Supplies On)
Drain leakage current when exposed to an overvoltage condition.

I_S (Fault—Power Supplies Off)
Source leakage current with power supplies off.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

THEORY OF OPERATION

The ADG438F/ADG439F multiplexers are capable of withstanding overvoltages from −40 V to +55 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs saturates, limiting the current. The current during a fault condition is determined by the load on the output. Figure 31 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of V_{SS} + 2.2 V to V_{DD} − 2.2 V (output loaded, 1 mA) is applied to the ADG438F/ADG439F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 270 Ω typically. However, when an overvoltage is applied to the device, one of the three MOSFETs saturates.

Figure 29 to Figure 32 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the n-channel MOSFET saturates because the voltage on the analog input exceeds the difference between V_{DD} and the n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET saturates because the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}). Because V_{TN} is nominally 1.4 V and V_{TP} − 1.4 V, the analog input range to the multiplexer is limited to V_{SS} + 1.4 V to V_{DD} − 1.4 V (output open circuit) when a ±15 V power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs remains off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET is at ground. A negative overvoltage switches on the first n-channel MOSFET, but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series remains off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions (power supplies off), the leakage current into and out of the ADG438F/ADG439F is limited to a few microamps. This limit protects the multiplexer and succeeding circuitry from over stresses as well as protects the signal sources that drive the multiplexer. Also, the other channels of the multiplexer are undisturbed by the overvoltage and continue to operate normally.

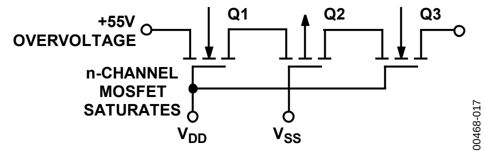

Figure 29. +55 V Overvoltage Input to the On Channel

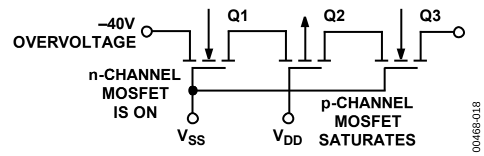

Figure 30. −40 V Overvoltage on an Off Channel with Multiplexer Power On

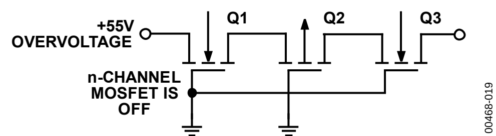

Figure 31. +55 V Overvoltage with Power Off

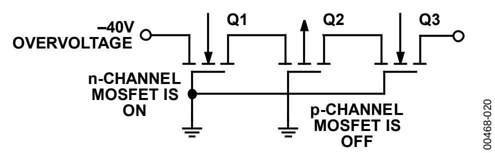

Figure 32. −40 V Overvoltage with Power Off

OUTLINE DIMENSIONS

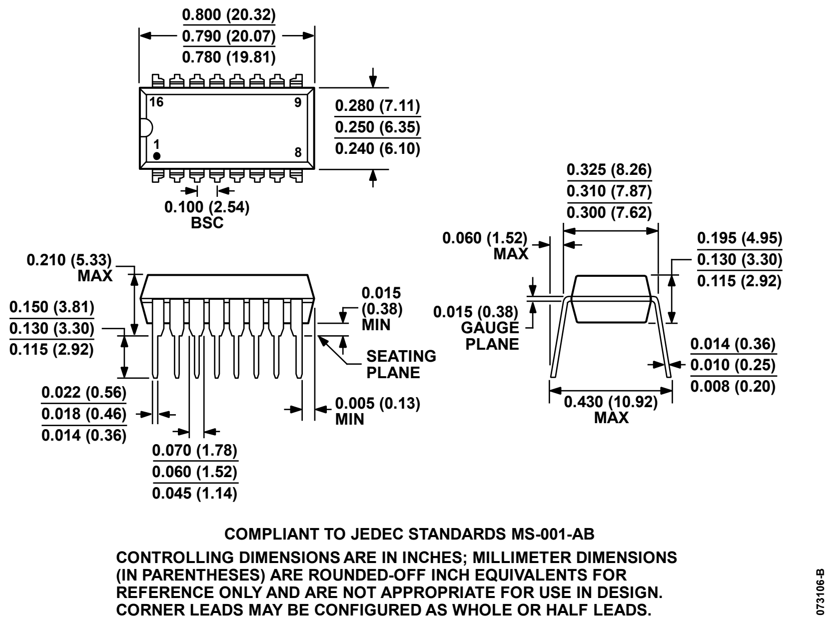

Figure 33. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)

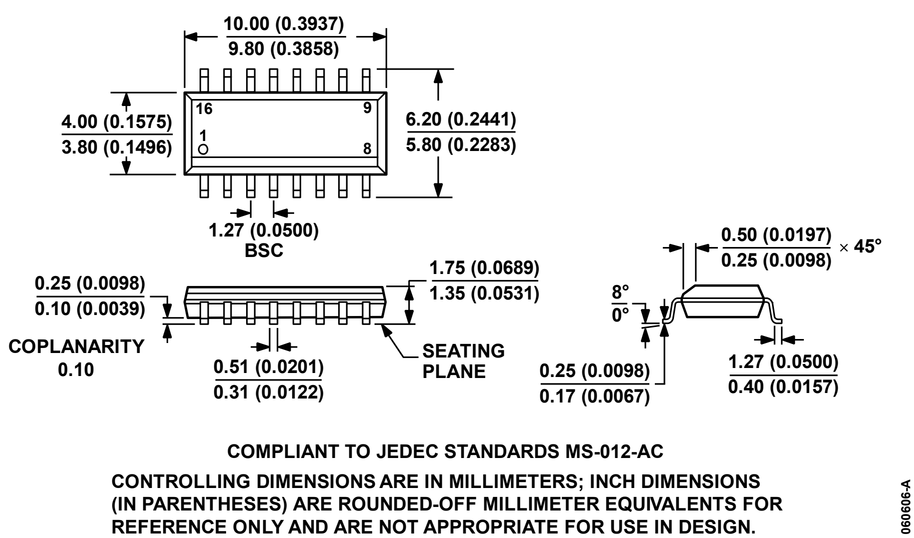

Figure 34. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

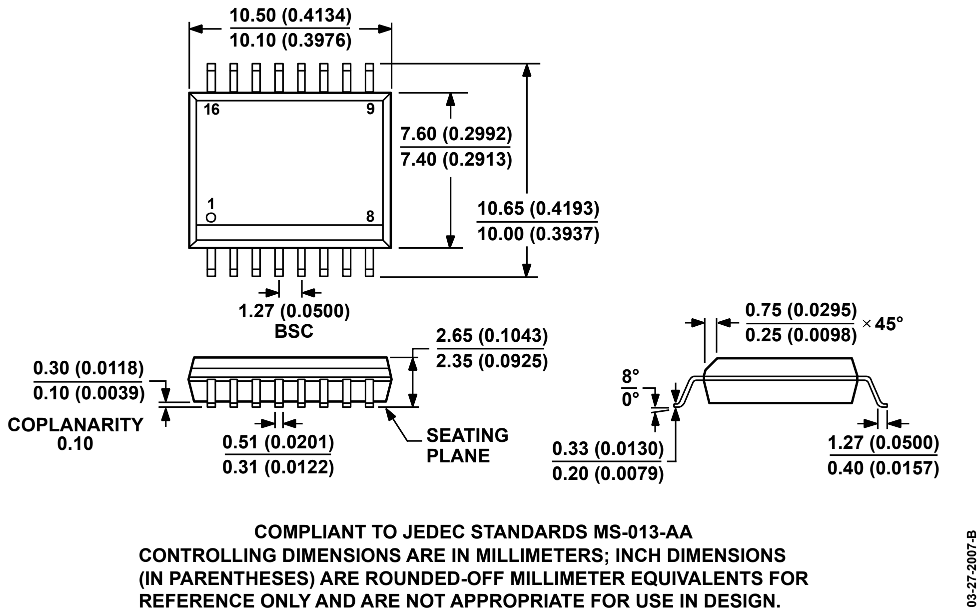

Figure 35. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG438FBN	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG438FBNZ	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG438FBR	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBR-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBRZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG438FBRZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBN	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG439FBNZ	−40°C to +125°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG439FBR	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBR-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBRW	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRWZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADG439FBRZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG439FBRZ-REEL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

[1] Z = RoHS Compliant Part.

NOTES